

100/15400

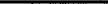


	Subclass
	Class

U.S. UTILITY Patent Application

PATENT NUMBER

JCT
GJ

 O.I.P.E. SCANNED <u>Hkm</u> ⁴ Q.A. 	PATENT DATE
--	--------------------

APPLICATION NO.	CONT/PRIOR	CLASS	SUBCLASS	ART UNIT	EXAMINER
09/757404		703	14	2123	Broda HOGAN

APPLICANTS

Steven Guccione
Scott McMillan
Brandon Blodget

Method and system for device-level simulation of a circuit design for a programmable logic device

PTO-2040

12/99

ISSUING CLASSIFICATION

WARNING:

The information disclosed herein may be restricted. Unauthorized disclosure may be prohibited by the United States Code Title 35, Sections 122, 181 and 368. Possession outside the U.S. Patent & Trademark Office is restricted to authorized employees and contractors only.

**Form PTO-436A
(Rev. 6/99)**

FILED WITH: DISK (CRF) FICHE CD-ROM
(Attached in pocket on right inside flap)

Best Available Copy

(FACE)